REMARKS

Claims 1-12 are pending and all have been rejected under 35 U.S.C. § 102(b). In response, Applicants are amending claims 1, 5, and 9, and respectfully submit that all pending claims 1-12 present subject matter that is patentable over the prior art of record, and, in view of the above amendments and following remarks, request that the Examiner reconsider the application.

REJECTIONS UNDER 35 U.S.C. § 102 - Frank

In paragraphs 2 and 3 of the Office Action, the Examiner rejected claims 1-12 under 35 U.S.C. § 102 (b) as being anticipated by U.S. Patent No. 5,297,265 to *Frank et al.*

The Examiner cited Fig. 5 and col. 11, line 22 through col. 12, line 68 to reject claims 1-12. In response, Applicants are amending claims 1, 5, and 9, and respectfully traverse.

Amended claim 1 recites:

> A method for managing memory in a computer system, comprising:
> for at least one memory page,
> dividing the page into a plurality of relocation blocks;
> placing the plurality of relocation blocks at a plurality of locations including one or a plurality of memory systems; and
> using a relocation table having a pluralities of entries to locate the relocation blocks at the plurality of locations;
> wherein, upon a memory access,
> using the relocation table to convert an address of the memory page to a relocation address of a relocation block containing the data intended for the memory access; and
> if the data intended for the memory access is not in physical memory, then loading, in physical memory, one or a plurality of relocation blocks containing the data related to the memory access.

Applicants respectfully submit that Applicants' claim 1 is patentably distinguished from *Frank*. *Frank*'s cited paragraphs from col. 11, line 12 to col. 12, line 68 disclose a page having subpages (col. 11, lines 23-26), and "[i]n data access

mode, . . . , the memory system attempts to satisfy that access by finding the subpage containing the data and returning it" (col. 11, lines 59-63). Even though *Frank* discusses "finding the subpage," *Frank* does not disclose, suggest, or make obvious *how* the sub pages are located. In contrast, claim 1 of the invention recites *how* to locate the relocation blocks by "using *a relocation table having a plurality of entries*" (page 16, claim 1, lines 6-7, emphasis added). Because *Frank* does not disclose, suggest, or make obvious a relocation table, *Frank* cannot logically disclose, suggest, or make obvious Applicants' additional claimed feature "using the relocation table *to convert an address of the memory page to a relocation address* of a relocation block" (page 16, claim 1, lines 8-10, emphasis added).

The Examiner also equates using *Frank*'s cache directories to using Applications' relocation table "to convert a memory page address to a relocation address' (Office Action, page 2, paragraph 3). As indicated above, Applicants' claimed relocation table and its entries are used to locate the relocation blocks, and the relocation table converts "an address of the memory page to a relocation address of a relocation block." In contrast, in *Frank*, "[e]ach cache directory is made up of descriptors. There is one descriptor for each page of memory in a cache" (col. 12, lines 22-24), "the descriptor records the associated SVA page address . . ." (col. 12, lines 27-28), etc. For the sake of argument, even if *Frank*'s caches directories are similar to Applicants relocation table having a plurality of entries, and *Frank*'s subpages are similar to Applicants' relocation blocks, *Frank* fails to teach, suggest, or make obvious using the cache directories to convert an address of a memory page to an address of a subpages. In fact, *Frank*'s cache directories record "associations between cache pages and SVA pages" (col. 12, lines 20-21).

Based on the relocation table and its entries, embodiments of Applicants' invention allow relocation blocks of a memory page to be at different locations, and,

as claimed in claim 1, the relocation blocks of a memory page are placed "at a plurality of locations including one or a plurality of memory systems," which is supported by Applicants' specification as "some of the blocks may be in physical memory, some other blocks may be in hard disc or other convenient locations including swap memory, [etc.,]" (page 11, lines 6-7). Further, upon a memory access, if the data intended for the memory access is not in physical memory, then claim 1 recites "loading, in physical memory, one or a plurality of relocation blocks containing the data related to the memory access." In contrast, *Frank*'s subpages do not afford such flexibility because "[e]ach page [that includes subpages] of SVA space is either *entirely* represented in the system or not represented at all" (col. 11, lines 27-29, emphasis added). In addition, even if information only in a subpage is accessed, the whole page must be loaded (col. 36, lines 53-55).

Because claim 1 recites limitations patentably distinguished from *Frank*, claim 1 is patentable.

Claims 2-4 depend directly or indirectly from claim 1 and are therefore patentable for at least the same reasons as claim 1. Claims 2-4 are also patentable for their additional limitations as appropriate.

Claims 5-8 and 9-12 recite limitations corresponding to claims 1-4, and are therefore patentable for at least the same reasons as claims 1-4.

SUMMARY

In conclusion, Applicants respectfully submit that pending claims 1-12 clearly present subject matter that is patentable over the prior art of record, and therefore request that the Examiner withdraw the rejections of the pending claims and pass the application to issue. If the Examiner has questions regarding this case, the Examiner is invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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